**IN THE CLAIMS**

Claims 2, 3 and 5 - 10 and 12 - 22 are pending in this application, wherein claim 13 is being amended and new claim 22 is being submitted for consideration, all as follows:

1. (Canceled).

2. (Previously Presented) A phase locked loop, comprising:

a phase-frequency detector that detects a phase difference between a reference signal introduced into a first input terminal and an input signal introduced into second input terminal, and that generates output pulses according to the phase difference;

a charge pump that outputs electric current according to an output signal from the phase-frequency detector;

a loop filter that attenuates a charge pump output of the charge pump;

a voltage controlled oscillator in which the frequency of an oscillator output signal is controlled according to an output voltage of the loop filter;

a programmable divider which divides the oscillator output signal from the voltage-controlled oscillator according to input division number data and feeds it back to the second input terminal of the phase-frequency detector;

a first modulator that transforms an incoming baseband signal into an integer signal for specifying a division number and that sends the integer signal to a control terminal of the programmable divider;

a second modulator which shapes the incoming baseband signal into a prescribed signal waveform and sends it to the voltage controlled oscillator; and

a controller which adjusts a phase error between the first modulator and the second modulator.

3. (Previously Presented) The phase locked loop according to Claim 2, wherein the charge pump and the controller are configured to change the loop bandwidth such that the loop bandwidth is broadened upon input of a signal to activate the phase locked loop, then convergence to a frequency occurs which depends on a constant representing a carrier frequency, and after a prescribed time, the loop bandwidth is narrowed.

4. (Canceled).

5. (Previously Presented) The phase locked loop according to Claim 2, wherein the first modulator further comprises:

a multiplier which multiplies the baseband signal by a constant;

a sigma delta circuit which carries out sigma delta modulation of output of the multiplier; and

an adder which adds a constant representing a carrier frequency to the output of the sigma delta circuit.

6. (Previously Presented) The phase locked loop according to Claim 2, wherein the first modulator further comprises:

a digital filter which transforms the baseband signal into a prescribed signal waveform;

a sigma delta circuit which carries out sigma delta modulation of the output of the digital filter; and

an adder which adds a constant representing a carrier frequency to the output of the sigma delta circuit.

7. (Original) The phase locked loop according to Claim 5, wherein the sigma delta circuit is a first order or second order sigma delta circuit.

8. (Original) The phase locked loop according to Claim 5, wherein the sigma delta circuit comprises a plurality of sigma delta circuits.

9. (Previously Presented) The phase locked loop according to Claim 2, wherein the first modulator comprises a multiplier that is structured to multiply the baseband signal by a constant;

a delta modulation circuit that is structured to carry out delta modulation of the output of the multiplier; and

an adder that is structured to add a constant representing a carrier frequency to the output of the delta modulation circuit.

10. (Previously Presented) The phase locked loop according to Claim 2, wherein the first modulator further comprises:

a digital filter which transforms the baseband signal into a prescribed signal waveform;

a delta modulation circuit which carries out delta modulation of the output of the digital filter; and

an adder which adds a constant representing a carrier frequency to the output of the delta modulation circuit.

11. (Canceled).

12. (Previously Presented) A data transmission circuit comprising:

a phase-frequency detector that detects a phase difference between a reference signal introduced into a first input terminal and an input signal introduced into second input terminal, and that generates output pulses according to the phase difference;

a charge pump that outputs electric current according to an output signal from the phase-frequency detector;

a loop filter that attenuates a charge pump output of the charge pump;

a voltage controlled oscillator in which the frequency of an oscillator output signal is controlled according to an output voltage of the loop filter; and

a programmable divider which divides the oscillator output signal from the voltage-controlled oscillator according to input division number data and feeds it back to the second input terminal of the phase-frequency detector,

a first modulator that transforms an incoming baseband signal into an integer signal for specifying a division number and that sends the integer signal to a control terminal of the programmable divider;

a second modulator which shapes the incoming baseband signal into a prescribed signal waveform and sends it to the voltage controlled oscillator;

an amplifier which is connected with the oscillator output of the voltage controlled oscillator in the phase locked loop; and

a control circuit structured to provide:

a loop bandwidth control signal to change the loop bandwidth of the phase locked loop, wherein the charge pump output current is changed in response to the loop bandwidth control signal;

an On/Off signal which turns on or off the amplifier; and

a reference signal and a baseband signal for the phase locked loop,

wherein the baseband signal incoming is amplified and outputted.

13. (Currently Amended) A method for providing a variable loop bandwidth phase locked loop comprising:

transforming in a first modulator that has a sigma delta circuit a baseband signal into an integer signal for specifying a division number;

sending the integer signal to a control terminal of a programmable divider;

shaping in a second modulator an incoming baseband signal into a prescribed signal waveform and that sends it to a voltage controlled oscillator;

sending an oscillation signal from the voltage controlled oscillator to the programmable divider;

providing a variable current charge pump which changes the loop bandwidth of the phase locked loop according to a control signal from a control circuit;

providing a phase-frequency detector for receiving a reference signal from a controller and the oscillator signal from the programmable divider;

~~inputting at an input a succession of "1" signals, wherein no modulated signal degradation occurs, and wherein even at a high symbol rate, the reference signal frequency remains low and sampling frequencies of the phase-frequency detector and the sigma delta circuit remain low;~~ and

adjusting a phase error between the first modulator and the second modulator.

14. (Original) The method for providing a variable loop bandwidth phase locked loop of claim 13 wherein the first modulator transforms a baseband signal into an integer signal for specifying a division number by:

multiplying in a multiplier a transmission pulse train by a constant;

transforming in the sigma delta circuit an output of the multiplier into a prescribed pulse train;

averaging in an averaging circuit an average of outputs from the sigma delta circuit in a given zone;

adding in an adder a constant representing a carrier frequency to the output of the averaging circuit; and

outputting a division integer to the programmable divider.

15. (Original) The method for providing a variable loop bandwidth phase locked loop of claim 13 wherein the first modulator transforms a baseband signal into an integer signal for specifying a division number by:

attenuating in a digital filter the baseband signal to a prescribed waveform;

transforming in the sigma delta circuit an output of the multiplier into a prescribed pulse train;

averaging, in an averaging circuit, an average of outputs from the sigma delta circuit in a given zone;

adding in an adder a constant representing a carrier frequency to the output of the averaging circuit; and

outputting a division integer to the programmable divider.

16. (Original) The method for providing a variable loop bandwidth phase locked loop of claim 13 wherein the first modulator transforms a baseband signal into an integer signal for specifying a division number by:

reading from a data table a transmission waveform which depends on the baseband signal;

introducing the transmission waveform into the sigma delta circuit;

transforming in a sigma delta circuit an output of the multiplier into a prescribed pulse train;

averaging in an averaging circuit an average of outputs from the sigma delta circuit in a given zone;

adding in an adder a constant representing a carrier frequency to the output of the averaging circuit; and

outputting a division integer to the programmable divider.

17. (Original) The method for providing a variable loop bandwidth phase locked loop of claim 13 wherein the second modulator comprises a pulse shaping circuit.

18. (Original) The method for providing a variable loop bandwidth phase locked loop of claim 17 wherein the sigma delta circuit provided comprises a first order sigma delta circuit for:

inputting an input signal x(n) which is output from the multiplier; and

outputting the integer signal from a quantizer which outputs an integer closest to a value of the input signal to an adder and to a delay circuit wherein the delay circuit adjusts a phase difference to eliminate phase error between the pulse shaping circuit and the adder.

19. (Original) The method for providing a variable loop bandwidth phase locked loop of claim 17 wherein the sigma delta circuit provided comprises a second order sigma delta circuit for:

inputting an input signal x(n) which is output from the multiplier;

outputting the integer signal from a quantizer which outputs an integer closest to a value of the input signal to an adder and to a delay circuit and a multiplier;

wherein the delay circuit adjusts a phase difference to eliminate phase error between the pulse shaping circuit and the adder;

and wherein a multiplier multiplies the output of the delay circuit by a constant.

20. (Original) The method for providing a variable loop bandwidth phase locked loop of claim 17 wherein the sigma delta circuit provided comprises:

using a plurality of stable sigma delta circuits which are lower than the second order level to make up a second order or higher-level multi-stage sigma delta circuit to assure stable operation.

21. (Previously Presented) The data transmission circuit according to claim 12, wherein the first modulator is not operating when the loop bandwidth control signal indicates a wider loop bandwidth of the PLL, and after the loop bandwidth signal changes the charge pump output current to narrow the PLL loop bandwidth, the first modulator

moves to an operation state and outputs the modulation signal according to the inputted baseband signal.

22. (New) A method for providing a variable loop bandwidth phase locked loop comprising:

multiplying in a multiplier a baseband signal by a constant;

transforming in a first modulator that has a sigma delta circuit the output of the multiplier into an integer signal for specifying a division number;

sending the integer signal to a control terminal of a programmable divider;

shaping in a second modulator an incoming baseband signal into a prescribed signal waveform and that sends it to a voltage controlled oscillator;

sending an oscillation signal from the voltage controlled oscillator to the programmable divider;

providing a variable current charge pump which changes the loop bandwidth of the phase locked loop according to a control signal from a control circuit;

providing a phase-frequency detector for receiving a reference signal from a controller and the oscillator signal from the programmable divider; and

inputting at an input of the multiplier a succession of the multiplier a succession of "1" or "0" based on the baseband signal, wherein the reference signal frequency is higher than the symbol rate. the sampling frequencies of the phase-frequency detector and the sigma delta circuit; and

adjusting a phase error between the first modulator and the second modulator.